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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/229,592	01/13/1999	BRIAN S. DOYLE	42390.P5578	5730

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	09/229,592	DOYLE ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 28-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 28-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/17/05 has been entered.

Claim Rejections - 35 USC § 103

2. Claims 1 – 12, 16, 29, 30, 32, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder et al. (USPAT 6063677, Rodder) in view of Sekine et al. (USPAT 5937300, Sekine) and (Jeuch et al. (USPAT 4939100, Jeuch).

Rodder discloses a method of forming a transistor in figures 3a – 5.

With regard to claim 1, Rodder discloses in figure 3a forming an alignment component (120 and 122) on a first portion of a substrate (102) of a semiconductor material. Rodder discloses in figure 3b and column 3, lines 5 – 40 depositing a silicide layer (106) over the substrate and on a second portion of the substrate adjacent to the alignment component. Rodder discloses in column 3, lines 5 – 40 forming the silicide layer by the salicidation (salicide or self-aligned silicide regions) process. Rodder further discloses in figure 3b wherein the two silicide regions substantially extend up to the alignment component on opposing sides of the alignment component. Rodder is silent

to steps in the salicide process such as depositing a metal layer over the alignment component and reacting the metal layer with the semiconductor material of the substrate, however, the salicide process includes these steps, is disclosed by Rodder, and is well known in the art. Sekine teaches in figures 13b – 13d the salicide process. Sekine teaches in figure 13b and column 2, lines 1 – 30 depositing a metal layer (813) over an alignment component (805, 804 and 810) and on a second portion (811) of a substrate (801) adjacent to the alignment component. Sekine further teaches in figures 13b – 13c and column 2, lines 1 – 30 reacting the metal layer with the semiconductor material of the substrate to form two silicide regions (814) substantially extending up to the alignment component on opposing sides of the alignment component. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the salicide process steps of Sekine to form the silicide regions in the method of Rodder in order to use a well known and highly understood method of forming the silicide layers that will reduce interconnect resistance of the polysilicon lines. Because of the use of the salicide process by Rodder, as disclosed in column 3, lines 5 – 40, it can now be seen that Rodder discloses depositing a metal layer over the alignment component and on a region of the substrate adjacent to the alignment component. Further because Rodder discloses in column 3, lines 15 – 16 that the raised source and drain regions are self aligned to the disposable gate and formed by the salicide process, it is obvious that the salicide regions of the combined method of Rodder and Sekine would produce silicide regions from reacting a metal layer with the semiconductor material of the substrate to form the two silicide regions substantially extending up to the alignment

component on opposing sides of the alignment component. Rodder discloses in figures 3e – 5 and column 5, lines 11 –26 replacing the alignment component with a conductive gate (112). Rodder teaches in figure 3f, doping the substrate in the first portion (channel 108) with channel dopants by a V_t implant. It is not clear in Rodder if the first and second portions have the same dopant type after the formation of the silicide regions and the replacement of the alignment component with the conductive gate, that is if the channel dopants are the same conductivity type as the starting substrate. Jeuch teaches in figures 6g – 6j, column 6, lines 18 – 22, and column 7, lines 7 – 21 wherein first (channel 58) and second portions (40, to either side of the first portion) of the substrate (40) having the same dopant type (P-type). It would have been obvious to one of ordinary skill in the art at the time of the present invention to have the same dopant type of the first and second portions of Jeuch in the method of Rodder in order to form a metal oxide semiconductor device (MOS or MIS) of n type wherein design characteristic for the specific circuit design, such as the required threshold voltage (V.sub.th), substrate dopant level, gate oxide thickness and gate electrode material are controlled partially through the channel dopant. Stated another way, it would have been obvious to use the dopant implant as taught by Jeuch (channel dopant of the same conductivity type as the starting substrate) for the channel dopant of Rodder figure 3F. Using this dopant step, the first and second portions of the substrate would have the same dopant type after formation of the silicide regions and the replacement of the alignment component with the conductive gate. As seen in Rodder figures 3G and 3H,

after the alignment component is replaced by the gate the only doped region in the substrate is region 108 which is the same dopant type as the substrate.

With regard to claims 2 – 4, Rodder discloses in columns 2 and 3, lines 59 – 67 and 1- 4 respectively that the alignment component includes silicon oxide which inherently posses the properties of being non-conductive, and in non-reactive with the metal layer when the metal layer is reacted with the semiconductor material of the substrate.

With regard to claims 5, 6 and 8, Rodder discloses in column 2, lines 11 – 17 that the alignment component is less than .10 microns wide. It is inherent that the alignment component has a thickness of between 1000/ and 2500/. It is inherent that the metal layer is between 300/ and 400/ thick.

With regard to claim 7, Sekine discloses that the metal layer includes titanium in column 2, lines 4 – 6.

With regard to claim 9, Sekine discloses in figure 13c that the silicide regions have lower surfaces located lower than a lower surface of the alignment component.

With regard to claim 10, Rodder discloses in figures 3c – 5 a method wherein the alignment component is removed. In figure 3c Rodder discloses depositing a layer (114) over the silicide regions and the alignment component. In column 3, lines 46 – 49 Rodder discloses planarizing the layer at least until the alignment component is exposed. In figures 3e– 5 Rodder discloses etching the alignment component at least until the substrate is exposed to leave an opening between inner surfaces of the silicide regions to allow for formation of the gate (112). It should be noted that inner surfaces of

the silicide regions substantially extending up to the alignment component on opposing sides of the alignment component, formed during the salicide process as shown in figures 13c - 13d of Sekine read on the claimed inner surfaces.

With regard to claim 11, it would be obvious in the method of Rodder, Sekine and Jeuch further comprising exposing the upper portions of the inner surfaces after the etching of the alignment component,. Because the alignment component and the upper portions of the inner surfaces are in contact (as shown in figures 13c – 13d of Sekine) as applied to claim 1, when the alignment component is removed, the upper portions of the inner surfaces would be exposed.

With regard to claim 12, Rodder discloses in columns 2 and 3, lines 59 – 67 and 1 – 52 respectively the alignment component and the layer are of different materials, one being of silicon oxide and the other being of silicon nitride.

With regard to claim 16, Rodder discloses in figure 4 forming doped regions (104) which extend from the silicide regions in underneath the gate. This step is disclosed as taking place after formation of the silicide regions and replacement of the alignment component with the conductive gate. See Rodder column 5 lines 42-45

Claims 29 and 32 are rejected similar to at least claims 4 and 9 – 12, respectively, with regard to Rodder, Sekine and Jeuch, above. It is inherent that the silicide regions form a Schottky junction.

With regard to claim 30, it is further obvious in the method of Rodder, Sekine and Jeuch that a portion of the metal layer above the alignment component is removed after

the metal layer is reacted with the semiconductor material of the substrate (see figures 13c – 13d of Sekine).

With regard to claim 33, Jeuch teaches in figures 6g and 6h, column 6, lines 18 – 22, and column 7, lines 7 – 21 wherein the first and second portions of the substrate are P-doped.

3. Claims 13 – 15 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder, Sekine, and Jeuch as applied to claim 1 above, and further in view of Inumiya et al. (USPAT 6054355, Inumiya).

With regard to claims 13, Rodder discloses in figure 5, and column 4, lines 56 – 67 depositing a gate dielectric layer (110), and forming a gate electrode on the gate dielectric layer. Rodder does not disclose forming a dielectric layer that would be sufficient in Rodder, Sekine, and Jeuch because the dielectric layer of Rodder would not insulate the entire upper portion of the inner surface of the silicide regions of Rodder, Sekine, and Jeuch. Inumiya teaches in figure 10g depositing a gate dielectric layer (116) lining the inside of a groove (114) formed by the removal of an alignment feature, and forming a gate electrode (117) on the gate dielectric layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the gate dielectric layer of Inumiya in the method of Rodder, Sekine, and Jeuch in order to form a gate insulating film and a gate electrode in a groove formed by the removal of an alignment feature.

With regard to claims 14 and 31, it is further obvious in the method of Rodder, Sekine, Jeuch, and Inumiya that the gate dielectric could be less than 10/ thick. The gate dielectric could be less than 10/ thick in order to facilitate the gate requirements for the decreasing dimensions of semiconductor devices.

With regard to claim 15, Rodder discloses that the gate electrode includes a metal in column 4, lines 64 – 67.

4. Claims 17 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder, Sekine, Jeuch, and Inumiya as applied to claims 1 and 13 above, and further in view of Gardner et al. (USPAT 6051865, Gardner).

With regard to claims 17 and 18, Rodder, Sekine, Jeuch, and Inumiya do not disclose using a high K dielectric layer. Gardner teaches in columns 3 and 4, lines 24 – 40 and 24-36 respectively a gate dielectric layer of barium strontium titanate that has a dielectric constant of at least 100. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the low K dielectric material of Gardner in the method of Rodder, Sekine, Jeuch, and Inumiya in order to decrease the transistor threshold voltage as stated by Gardner in column 3, lines 26 – 33.

With regard to claim 19, Rodder, Sekine, Jeuch, Inumiya and Gardner do not disclose using platinum as a gate electrode. It is well known in the art to form a gate electrode of platinum. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the platinum gate electrode in the process of

forming a transistor of Rodder, Sekine, Jeuch, Inumiya and Gardner in order to use a low-resistivity conductor for the gate material.

5. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder, Sekine, and Jeuch as applied to claim 1 above, and further in view of Wolf (Silicon Processing for the VLSI ERA, Vol. 2).

Rodder, Sekine, and Jeuch obviously disclose that the silicide regions extend partially below the alignment component because that is a property of the silicide process as disclosed by the references. Rodder, Sekine, and Jeuch do not disclose that the metal layer includes nickel. Wolf teaches on pages 146 a salicide formed from nickel. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the cobalt salicide of Wolf in the method of Rodder, Sekine, and Jeuch in order to create a silicide that exhibits lower resistivities as taught by Wolf on page 146.

Response to Arguments

6. Applicant's arguments filed 2/17/05 have been fully considered but they are not persuasive.

Applicant has argued that neither Rodder, Sekine, nor Jeuch teach the first and second portions of the substrate having the same dopant type after formation of the silicide regions and replacement of the alignment component. This is not persuasive. First, the primary reference, Rodder, teach forming their substrate doped source/drain

regions 104 (as shown in figure 4) after forming the silicide regions and replacement of the alignment component. Rudder does not explicitly disclose the first portion (channel portion 108) having the same dopant type as the starting substrate. Rudder is silent as to the dopant type of the first portion 108 such that is it not clear whether the first and second portion have the same dopant type before doping the source/drain regions 104. Jeuch teach a channel implant to adjust the threshold voltage of the device. This channel implant is similar to that of Rudder, but Jeuch teach that it is the same conductivity type as the starting substrate. Thus, using the definite teaching of the channel implant being the same conductivity type as the starting substrate of Jeuch in the process of Rudder, one clearly sees that the combined references teach the first and second portions having the same conductivity type after formation of the silicide regions and replacement of the alignment component. The fact that the Rodder teach later doping the substrate to form source/drain regions 104 has no bearing on the claim as written because claim 1 does not preclude later process steps such as doping the source/drain regions. Immediately after forming the silicide regions and replacement of the alignment component the first and second regions have the claimed same dopant type and thus render the claims obvious.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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